WHAT IS CLAIMED IS:

1. An information processing apparatus comprising:

a deciding unit that decides whether a given instruction exists within a predetermined instruction set;

a first operating unit that executes the instruction when the deciding unit decides that the instruction exists within the predetermined instruction set;

a structure information output unit that outputs structure information for determining a circuit structure to execute the instruction when the deciding unit decides that the instruction does not exist within the predetermined instruction set; and

at least one second operating unit that executes the instruction in the circuit structure determined based on the structure information output from the structure information output unit.

2. The information processing apparatus according to claim 1, wherein the second operating units are provided in plurality.

3. The information processing apparatus according to claim 1, wherein when the deciding unit decides that the instruction does not exist within the predetermined instruction set, the structure information output unit selectively outputs structure information for determining the circuit structure to execute the instruction, from among pieces of structure information.

4. The information processing apparatus according to claim 3, wherein the structure information output unit selectively outputs structure information for determining the circuit structure to execute the instruction from among the structure information, based on any one of an address assigned by the instruction and an address held in a predetermined register or both.

5. The information processing apparatus according to claim 1, further comprising a rewritable memory for storing the structure information.

6. The information processing apparatus according to claim 5, wherein in addition to the memory, the structure information is stored in a predetermined field within the instruction or in a predetermined register.

7. The information processing apparatus according to claim 6, wherein each time when the second operating unit executes the instruction, a value held in the predetermined register is updated based on the structure information held in the memory.

8. The information processing apparatus according to claim 5, wherein the instruction includes an instruction that instructs to load the structure information into the memory.

9. The information processing apparatus according to claim 5, further comprising:

a second deciding unit that decides whether the instruction is an instruction to load the structure information into the memory when the deciding unit decides that the instruction does not exist within the predetermined instruction set; and

an instruction issuing unit that issues a plurality of instructions to load the structure information into the memory, when the second deciding unit decides that the instruction is the instruction to load the structure information into the memory, wherein

the first operating unit executes the instruction issued by the instruction issuing unit.

10. The information processing apparatus according to claim 5, further comprising:

a second deciding unit that decides whether the instruction is an instruction to load the structure information into the memory when the deciding unit decides that the instruction does not exist within the predetermined instruction set; and

an instruction issuing unit that issues an instruction to transfer the structure information to a predetermined register to which memory is allocated, when the second deciding unit decides that the instruction is the instruction to load the structure information into the memory, wherein

the first operating unit executes the instruction issued by the

instruction issuing unit.

11. The information processing apparatus according to claim 5, further comprising:

a second deciding unit that decides whether the instruction is an instruction to load the structure information into the memory when the deciding unit decides that the instruction does not exist within the predetermined instruction set; and

an instruction issuing unit that issues an instruction to store the structure information in a predetermined area within an address space to which the memory is allocated, when the second deciding unit decides that the instruction is the instruction to load the structure information into the memory, wherein

the first operating unit executes the instruction issued by the instruction issuing unit.

12. The information processing apparatus according to claim 5, further comprising:

a second deciding unit that decides whether the instruction is an instruction to load the structure information into the memory when the deciding unit decides that the instruction does not exist within the predetermined instruction set; and

an instructing unit that instructs a DMA controller to transfer the structure information to the predetermined area within the address space to which the memory is allocated, when the second deciding unit

decides that the instruction is the instruction to load the structure information into the memory.

13. The information processing apparatus according to claim 1, wherein the second operating unit replaces optional bits within given data, in the circuit structure determined based on the structure information output from the structure information output unit.

14. The information processing apparatus according to claim 1, wherein the second operating unit counts the number of 1s within given data, in the circuit structure determined based on the structure information output from the structure information output unit.

15. The information processing apparatus according to claim 1, further comprising a selecting unit that outputs only information at a predetermined bit position within the structure information output from the structure information output unit.

16. An information processing method comprising:

deciding whether a given instruction exists within a predetermined instruction set;

a first step of executing the instruction when it is decided at the deciding that the instruction exists within the predetermined instruction set;

outputing structure information for determining a circuit structure

to execute the instruction when it is decided at the deciding that the instruction does not exist within the predetermined instruction set; and

a second step of executing the instruction in the circuit structure determined based on the structure information output at the outputting.

17. The information processing method according to claim 16, wherein when it is decided at the deciding that the instruction does not exist within the predetermined instruction set, then at the outputting, structure information is selectively output for determining the circuit structure to execute the instruction, from among pieces of structure information.

18. The information processing method according to claim 17, wherein at the outputting, the structure information is selectively output based on at least one of an address assigned by the instruction and an address held in a predetermined register.

19. The information processing method according to claim 16, wherein the structure information is held in a rewritable memory.

20. The information processing method according to claim 19, wherein the structure information is held in a predetermined field within the instruction or in a predetermined register in addition to the memory.

21. The information processing method according to claim 20,

wherein each time when the instruction is executed at the second step, a value held in the predetermined register is updated based on the structure information held in the memory.

22. The information processing method according to claim 19, further comprising:

a third step of deciding that includes deciding whether the instruction is an instruction to load the structure information into the memory when it is decided at the deciding that the instruction does not exist within the predetermined instruction set; and

issuing a plurality of instructions to load the structure information into the memory when it is decided at the third step that the instruction is the instruction to load the structure information into the memory, wherein

at the first step, the instruction issued at the issuing is executed.

23. The information processing method according to claim 19, further comprising:

a fourth step of deciding whether the instruction is an instruction to load the structure information into the memory when it is decided at the deciding that the instruction does not exist within the predetermined instruction set; and

issuing an instruction to transfer the structure information to a predetermined register to which the memory is allocated when it is decided at the fourth step that the instruction is the instruction to load

the structure information into the memory, wherein

at the first step, the instruction issued at the issuing is executed.

24. The information processing method according to claim 16, further comprising outputting of only information at a predetermined bit position within the structure information output at the outputting.